

Program-Controlled High-Voltage Pulse Generator for Ion Beams Source

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Abstract – Designed in the Nuclear Physics Institute a vacuum arc source of plasma and accelerated ions “Raduga-5” [1] can be used for materials modification by various methods (plasma sputtering, ion implantation, combined methods of treatment). The group of technical solutions used at “Raduga-5” design allow to vary in the wide range the plasma concentration and the ion beam current density. But it must be noted the reaction pattern of the source on the load for the control of high voltage pulsed generator (HVPG). In a particular case we can consider the load as plasma filled diode. When we use the linear law of high voltage pulses generation control the unjustified energy deposition appears at the source elements by episodically current overloads. There is also a probability of essential voltage exceeding at the power system elements at the instant load resistance increase (arc discharge breakdown in the plasma and ions source).

1. Introduction

This publication is dedicated to the control scheme design of HVPG of the “Raduga-5” installation, new in principle. For solving this task the starting pulses generation with smooth increase to the operating frequency and simultaneous load current control has been proposed. At a definite number of overload pulses from the current sensor a smooth frequency decrease is carried out. By long duration of the power supply overload it is disconnected from the power circuit. The starting pulse generator is based on the micro controller AVR of the AT90S2313 Amtel micro controller [2–5] and represents program realized DDS (Direct Digital Synthesizer). It is intended for programmed time interval and logical HVPG control signals generation.

2. Power Source Description

The scheme of program controlled driving pulses former is given in Fig. 1.

AT90S2313 micro controller consists of the following devices: a programming analog comparator, two programming controlled timers/counters (8 and 16 digit), two I/O ports (8 digits B port and 7 digits D port), a built-in quartz synchronizing clock, a universal anisochronous transceiver UART for outer driving computer connection, an electrically erased memory for program (FLASH) and data (EEPROM).

The analog comparator allows to compare the voltage values, applied to two micro controller inputs. In our case they are: 1 – the signal of HVPG overload and 2 – the magnitude of guard current setting. As a overload signals sensor the current transformer (CT) is used. It is inserted in the primary supply-line three-phase transformer circuit of the HVPG. The straightened CT signal comes to the analog current comparator. The overload current control is carried out by the pulse-length modulation (PLM) which is program realized. For this purpose PLM base voltage is applied to the second comparator input which determines the peak overload current. This voltage is formed by micro controller with assistance of the built-in timer operating in the 8 bit PLM mode. For the PLS signal filtration two-section low-pass filter R1, C1, R2, C9, R10. Simultaneously the resistors form the divider which determines the current regulation scale. In this case the maximum peak current corresponds to the code of 255 50.11 A is chosen that corresponds to the voltage of 0.511 V on the current sensor. Taking into account the fact that the constant component at the PLM output varies from 0 to 5 V, the necessary division coefficient is about 9.7.

For the control of HPVPG pulses generation and blocking his performance the transistor switch is connected to the B port output. The applied field-controlled transistor of IRL734N type can switch the current about 20 A with minimal losses. To leave the transistor closed during the “Clean” signal of the micro controller (the ports at this time are in high impedance state) between gate and source the resistor R11 is switched on. For gate capacity recharge current limiting the resistor R10 is switched on.

For the on-line information display the liquid-crystal panel (LCP) with built-in controller is used. Using the standard 14-pin connector LCP exchange data with driving micro controller (with AVR in our case). The AVR microcontroller sends instructions to the LCP which controls their operation modes and ASCII codes of the displayed symbols.

The LCP connection is realized in the following way: the control signals E and RS are formed program with a fixed time delay at the AVR I/O lines, the W signal is fixed in the direction of the transfer from AVR to LCP. In the given example the data bus consists of 4 digits. Each data byte is transmitted during two serial sending starting from the high-order quaternion. The 3×4 keyboard connection providing the state

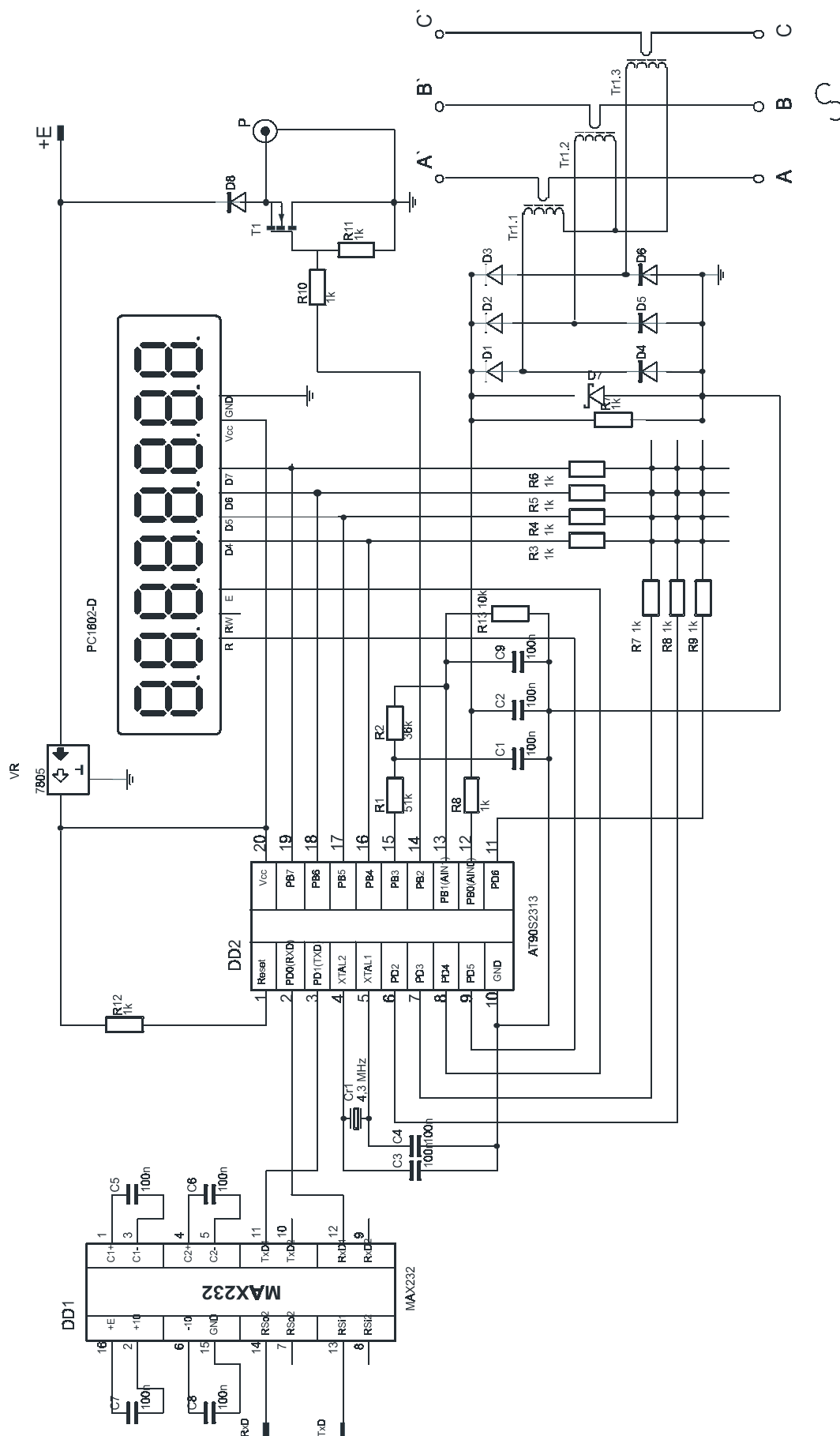


Fig. 1. Program controlled Pulsed High Voltage Generator

inquiry is carried out by the combined scheme. Four keyboard columns are connected to the low-order quaternion of B port, and three rows – to the D port lines. The same 4 D port digits transmit the control data to the LCP port. When using the B port lines it is necessary to consider precautions. As they used in the both ways it is necessary to foresee the impossibility of LCP segment lines shunting. For this purpose the current-limiting resistor is switched on in each line of the keyboard matrix sequentially. The use of built-in tightened resistors at the input reduces the number of external components. The choice of R1–R8 resistors values is based on the consideration that the voltage dropping on them when the keys are pressed is rather low. Under the values indicated at the scheme and the supply voltage of 5 V the logical levels are 0.6 V for “0” and 4.95 V for “1”. Thus, these outlets realize two functions: data output for LCP and data input during keyboard inquiry. It is because due to high settings flexibility of the I/O ports. Before each scan stroke of the indicator the port configuration changes. Firstly one quadruple the tighten resistors inputs (columns) connection and second logical “0” setting at the other outputs triplet (rows) for the column definition with pressed key, and then conversely for the row definition with pressed key. The pressed key code corresponds to obtained sum of values in the conversion table. Between each state change the short delay is entered for level settings on the port lines. The use of this method is more efficient comparing with the single-line scanning method relatively to the code compactness. During the commutation process the indicator is switched off and by keyboard inquiry finishing the ports configuration is ready to dynamic indicator control. The main service functions are programmed through the keyboard.

The EEPROM of electrically erased AVR data memory is intended for energy-independent data storage, which can change at the object immediately. These are calibration coefficients, various presets, system configuration parameters etc. The EEPROM memory can be both read and write by the program way. But there are no special commands for call to EEPROM memory. Therefore reading and writing of

the EEPROM cells are carried out through I/O registers (EEAR – address register, EEDR – data register, EECR – control register).

For external controlled computer connection the RS-232 interface is used built on the D1 (MAX232) chip. The T×D micro controller signal is led out to the PD2 port line, the micro controller receiving signal is led out to the PD1 port line.

The main process runs practically continuously and is interrupted only at 5.127 ms (21 cycles) at each 1 ms for variables upgrade containing the information about the real system status. It consists of three sections: RESET (spill processing), FREQUENCY SETTING (the current frequency setting and guard settings) and HOUSEKEEPING (service functions).

The generator can be also used with any automated control systems, performing the function of logical programming duration signal former, or pulse generator functions (series or continuous sequence).

The generator parameters are the following:

Range of the generated frequencies, Hz	50–250
The controlled pulses duration, ms	1–100
The frequency setup step, Hz	1
Output voltage, V	5
10 frequency fore settings	
The inner reprogramming regime	
The possibility to control through RS-232 channel	

References

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